REMARKS

Examiner has rejected claims 1 through 3, 5 through 18 and 21 through 30 under 35 U.S.C. § 103 (a) as being unpatentable over USPN 5,978,578 (Azarya). Examiner has rejected claims 4, 16 through 18 and 31 through 41 under 35 U.S.C. § 103(a) as being unpatentable over Azarya in view of USPN 5,903,737 (Han). Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Azarya. Applicant respectfully traverses the rejections and respectfully requests reconsideration.

Azarya discloses an openbus system for control automation networks. Han discloses an apparatus and method for serial data communication utilizing general microcomputer.

The references, whether considered alone or in combination, do not disclose or suggest the subject matter set out in the claims of the present application.

For example, independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The network device includes a host processor. The chip includes a media access controller, a host interface and an embedded processor. This functionality is not disclosed or suggested by the cited art.

Examiner has asserted that this functionality is disclosed by Figure 4 of Azarya. This is clearly not the case.

For example, claim 1 sets out that the media access controller is connectable to the computer network. The media access controller provides the chip with access to the computer network independent of a host processor. This is not disclosed or suggested by Azarya.

Examiner has asserted that Figure 4 of Azarya shows a media access controller connectable to computer network 18 and providing access to network 18 independent of a host processor. Since network interface card (NIC) 24 is the only entity within open node controller 10 that is connected to network 18, Examiner appears to be arguing that NIC 24 is a media access controller.

However, a person of ordinary skill in the art would recognize network interface card (NIC) 24 is not a media access controller. NIC 24 is a card that provides interface to a network. As is recognized by persons of ordinary skill in the art, a media access controller, is an entity used to implement a particular layer of protocol within a particular network protocol. For example, a MAC Layer specifies fair and deterministic access to the medium, address recognition and generation and verification of frames. See for example, Azarya at column 17, lines 17 through 41.

Likewise, claim 1 sets out that the host interface is connectable to the host processor. Examiner has asserted that Figure 4 contains a host interface. However, it is difficult to ascertain which entity within Figure 4 of Azarya Examiner regards as a host interface and which entity Examiner regards as a host processor.

Applicant notes that the development system 180 cannot qualify as a host processor because *development system 180 is connected to openbus node controller 10 via network 18, and not by a separate host interface.* See Figure 3 and Azarya at column 8, lines 63 through 65.

Since development system 180 communicates to openbus node controller 10 via network 18, it is clear that openbus node controller 10 does not include a separate host interface.

Interface circuitry boards 20 do not function as a host interface as these do not interface to a host processor, but rather to sensors and I/O devices 26.

Claim 1 also sets out an embedded processor coupled between the host interface and the media access controller. This is not disclosed or suggested by Azarya. Open node controller 10 includes an embedded processor 22; however, embedded processor 22 is not coupled between a host interface and a media access controller. As discussed above, openbus node controller 10 does not include a host interface or a media access controller.

Claim 1 also sets out that the embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. This is not disclosed or suggested by Azarya. As discussed above, openbus node controller 10 does not include a host interface and embedded processor 22 does not communicate with a host interface.

Claim 1 also sets out that the embedded processor is programmable to send the manageability information to the media access controller for transmission over the computer network. This is not disclosed or suggested by Azarya. As discussed above, openbus node controller 10 does not include a media access controller and embedded processor 22 does not send information to a media access controller.

Similarly, independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. This functionality is not disclosed or suggested by the cited art.

As discussed above, Figure 4 of Azarya does not disclose a media access controller. A person of ordinary skill in the art would recognize network interface card (NIC) 24 is not a media access controller. It is a card that provides interface to a network. As is recognized by persons of ordinary skill in the art, a media access controller, is an entity used to implement a particular layer of protocol within a particular network protocol. For example, a MAC Layer specifies fair and deterministic access to the medium, address recognition and generation and verification of frames. See for example, Azarya at column 17, lines 17 through 41.

Also, Azarya does not disclose an interchip communications interface interchip communications interface connected to an interchip communications means.

Likewise, claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. This functionality is not disclosed or suggested by the cited art.

As discussed above, Azarya does not disclose a single chip that includes a media access controller and an embedded processor. As discussed above, Figure 4 of Azarya does not disclose a media access controller. A person of ordinary skill in the art would recognize network

interface card (NIC) 24 is not a media access controller. It is a card that provides interface to a network. As is recognized by persons of ordinary skill in the art, a media access controller is an entity used to implement a particular layer of protocol within a particular network protocol. This is not the same as a network interface card.

Similarly, independent claim 31 sets out a method of managing a network device including a host processor, an I^2C bus, and an I^2C-compliant device. In a first step of claim 31, a media access controller is used to receive network manageability information requests from a computer network. The media access controller communicates with the computer network independent of the host processor and the I^2C-compliant device. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya nor Han disclose or suggest using a *media access controller* to receive *network manageability information requests* from a computer network.

In a second step of claim 31, the I^2C bus is used to obtain network manageability information about the I^2C-compliant device. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya nor Han disclose or suggest using a I^2C bus to obtain network manageability information about a I^2C-compliant device.

In a third step, of claim 31, the media access controller is used to place the manageability information on the computer network. This is not disclosed or suggested by Azarya or Han. Particularly, neither Azarya nor Han disclose or suggest using a media access controller to place manageability information on a computer network. As discussed above, Figure 4 of Azarya does not disclose a media access controller. A

person of ordinary skill in the art would recognize network interface card (NIC) 24 is not a media access controller. It is a card that provides interface to a network.

Since none of the steps of claim 31 are disclosed or suggested by Azarya or Han, whether considered alone or in combination, Applicant respectfully traverses the rejection under 35 U.S.C. § 103(a) and respectfully requests reconsideration.

Applicant notes that implementation of a web server chip, as set out in the claims of the present case, allows for implementation of network management at significantly reduced costs than is provided by prior art systems. Applicant believes that this invention is a significant, non-obvious improvement over prior art systems.

Response to New Arguments by Examiner

Examiner has argued that it would have been obvious to a person having ordinary skill in the art to provide the system of Azarya in a chip. This is clearly not the case.

The system of Azarya is significantly more complex than the functionality Applicant claims to put upon a chip. The openbus node controller 10 includes a plurality of interface circuitry boards 20, an embedded processor 22, a network interface card 24 and a bus. The task of placing all this functionality within a single chip would be daunting and certainly not an obvious matter for a person of ordinary skill in the art. For example, Azarya indicates the interface circuitry boards 20 can be any widely available off the shelf third party automation control I/O board designed for either generic or specific applications. Reducing any one of

these boards to a single chip would be daunting in itself. But to take a plurality of these automation control I/O boards and put them on a single chip along with a network interface card and embedded processor would be an extremely difficult task. There would be a very high number of I/O pins that would be necessary for such a chip. There would be significant power issues and heat dissipation issues to be overcome in implementing the I/O for such a chip. If this is a possible task, it would surely not be an obvious one for a person of ordinary skill in the art.

In order to obtain modify the Azarya to obtain the subject matter of the present invention, it would first be necessary to completely redesign the functionality of openbus node controller 10 to accomplish the functionality set out by the claims of the present case. It is doubtful that after the redesign any of the original functionality of the subject matter disclosed by Azarya would remain. In any event, the resulting functionality would be completely incompatible with the openbus system set out in Azarya. Having completely redesigned the functionality of the controller, it would then be possible to place the redesigned functionality on a single chip. However, this would clearly be a case of hindsight reconstruction from the present application and not something that would in any way be obvious to person of ordinary skill in the art without the goal of reconstructing the claimed subject matter of the present application.

Examiner has also asserted that in column 10, line 63 through column 11, line 5, Azarya discloses a media access controller to receive network manageability information requests from a computer network.

This is clearly not the case. Column 10, line 63 through column 11, line 5 of Azarya reads as follows:

> The first step of the network communication management process is to wait for a network communication (step 78). Once a network communication is received, the processor checks if it is a network message (step 80). If it is not a network message control returns to step 78. If it is a network message, the message is then analyzed (step 82) and the dispatcher is activated (step 84). Note that optionally, the network communication management process can be implemented in Java code. The dispatcher is described in more detail below.

This section of Azarya does not mention a media access controller or a reception of network manageability information requests.

Applicant believes the present case in condition for allowance and favorable action is respectfully requested.

Respectfully submitted,
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